IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/196,396, filed July 15, 2002, ~~pending~~ now U.S. Patent 6,614,003, issued September 2, 2003, which is a continuation of application Serial No. 09/892,156, filed June 26, 2001, now U.S. Patent 6,420,681, issued July 16, 2002, which is a continuation of application Serial No. 09/618,885, filed July 18, 2000, now U.S. Patent 6,329,637, issued December 11, 2001, which is a continuation of application Serial No. 09/145,832, filed September 2, 1998, now U.S. Patent 6,121,576, issued September 19, 2000.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] A test apparatus for evaluating circuit performance of the semiconductor package 10 is shown as including an insert 16 and a substrate member 18. The insert 16 is noncompliant and is typically formed of ceramic or silicon with a pattern of electrical contact sites 20 micromachined on its upper surface 22. The contact sites 20 may comprise simple planar pads, or contact pockets of any configuration, as explained infra. The contact sites 20 are connected by conductive traces, not visible, to bond pads 24, the latter being connected by wire bonds 26 to conductive traces 28 on the substrate member 18. The wire bonds 26 and conductive traces 28 on the insert 16 and substrate member 18 may be encapsulated in resin for protection. Other means for connecting the contact sites 20 to a controller conducting a test, burn-in, etc. may be used, as known in the art.

Please replace paragraph number **[0052]** with the following rewritten paragraph:

[0052] In drawing FIG. 6, several types of BGA contact sites 20 are shown as examples illustrating the wide variety of solder ~~bumps/balls12~~ bumps/balls 12 and contact sites 20 combinations whose temporary connection is enhanced by use of an elevated submelting

softening temperature T_s. Each solder bump/ball 12 attached to semiconductor package 10 is configured to be in compressive conductive contact with a contact site 20.